Question 1 - QCM:
Single Electron Transistors

The SET is a discrete charge device using three conductive nanodots as source, drain and gate and with thin tunneling oxides between central island and the source and the drain, operating under the orthodox theory of Coulomb blockade. Choose the correct properties of this family of devices:

1. A SET inverter can be built with two identical SETs, in contrast with a CMOS inverter that needs one n-type and one p-type MOSFET. This is due to the fact that an SET shows both positive and negative transconductance, depending on the applied gate voltage.

2. SET logic is a wireless logic.

3. The Id-Vd output characteristic of a SET transistor saturates because of the Coulomb blockade effect.

4. The effect of background charge on a SET affects the values of its threshold voltages.

5. The PADOX technology for SETs uses metal (like Al) dots and SiO2 as a tunneling dielectric.

6. With a metallic central island of around 2nm in diameter, one can obtain a Coulomb blockade effective at room temperature (T=300K).

7. A SET inverter consumes static power in logic 1 and logic 0 states which is contrary to the behavior of a CMOS inverter.

8. The SET can be used as an ultra-high sensitive elementary charge detector.

9. In a SETMOS hybrid device the period of the oscillations is independent of the amplification of the current provided by the MOSFET device.

10. The intrinsic frequency operation (speed) of SETs is limited to kHZ to MHz range due to their very low currents (typically less than nAs).

Question 2 - SET

Answer in the following six (6) questions:

1. **Describe** the electronic operation principle of a Single Electron Transistor (SET) and the basics of the orthodox theory and Coulomb blockade. **Discuss** the related performance motivation for developing such device and expected performance as electronic switch (at least the consumption and the frequency of operation). Explain why the SET is not a true quantum device.
2. **Enumerate** and **motivate** at least **three (3) major advantages** of an SET electronic switch compared to a conventional MOSFET.
3. **Enumerate** and **motivate** at least **three (3) major disadvantages** of an SET electronic switch compared to a conventional MOSFET.
4. **Provide and describe three (3) examples of SET technological implementations based on various ideas and material systems**. **Discuss and comment** the specific merits and drawbacks of the resulting SET electrical characteristics in the selected implementations. Would the room temperature operation be achievable?
5. **Enumerate and discuss** some of the major challenges that should be still addressed at technology scaling and design levels for SETs for a full industrial take-up. **Discuss** the merits of a hybrid SET-CMOS technology and IC design compared to conventional CMOS and pure SET-based circuit design.
6. **Enumerate and motivate three (3) major fields of potential electronic applications of SET devices**, taking into account their specific merits and limitations.

1. Basic principles of SET and 'orthodox' theory are the lecture slides.
2. Three major advantages of SET versus MOSFET switch:
- ultra low power operation at sub nA current and tens of mV voltages.
- same device can be used as both n- and p-type switch
- adds new functionality to analog applications (due to its periodic oscillations characteristics)
3. Three major disadvantages of SET versus MOSFET switch:
- room temperature operation is prohibited by required scaling dowm to around 1nm of the the central island (need cryogenic operation of dimensions of around 10nm)
- high sensitivity to backgorund charge (needs parasitic charge-free technology)
- low on currents involve low frequency operation
4. Three technological implementation:
- metal (Al) dots separated by Al2O3 oxides
- Padox of V-Padox using silicon nanowires and their controlled oxidation on SOI substrates
- Gate All Around (GAA) Silicon nanowire with triangular cross section and formation of SET islands in the corners.
5. technology challenges for SETs:
- technology scaling down to nm and control of variability of island
- background charge control
- low speed IC limitations
Merits of hybrid SET-CMOS:
- new analog functionality
- interfaces fro quantum applications
6. Fields of applications:
- charge sensors
- ultra low power cryogenic technology
- readout electronics for spin qubits